Thinkcore TC-RK3568
Stamp Hole Development Board
Specification

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Release Note

Version	Date	Author	Description
Rev.01	2022-08-04	ThinkcoreMan	Revision

Technical support

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Catalogue

Chapter 1. TC-RK3568 Stamp Hole Development Board Introduction

1.1 TC-RK3568 Stamp Hole Development Board Brief

TC-RK3568 Stamp Hole Development Board includes TC-RK3568 Stamp Hole SOM and carrier baord.

TC-RK3568 Stamp Hole system on module is equipped with Rockchip 64-bit processor RK3568 which is configured with dual-core GPU and high-performance NPU.

RK3568, the quad-core 64-bit Cortex-A55 processor, with 22nm lithography process, has frequency up to 2.0GHz, delivering efficient and stable performance for data processing of back-end equipment. There are a variety of storage options, allowing customers to quickly implement the research and production of products. It supports up to 8GB RAM, with up to 32Bit width and frequency up to 1600MHz. It supports all-data-link ECC, making data safer and more reliable, and meeting the requirements of running large-memory products application. It is integrated with dual-core GPU, high-performance VPU and high-efficiency NPU. The GPU supports OpenGL ES3.2/2.0/1.1, Vulkan1.1. The VPU can achieve 4K 60fps H.265/H.264/VP9 video decoding and 1080P 100fps H.265/ H.264 video encoding. The NPU supports one-click switching of mainstream frameworks like Caffe/TensorFlow.

With MIPI-CSI x2, MIPI-DSI x2, HDMI2.0, EDP video interfaces, it can support up to three screen output with different display. The built-in 8M ISP supports dual cameras and HDR. Video input interface can be connected to an external camera or multiple cameras. It is equipped with dual adaptive RJ45 Gigabit Ethernet ports, through which internal and external network data can be accessed and transmitted, improving network transmission efficiency, and meeting the needs of products with multiple network ports such as NVR and industrial gateway.

The carrier board includes many interfaces, such as 4G LTE Port, USB3.0, USB2.0, PCIE, dual Ethernet, WIFI, Bluetooth, Audio input and output, HDMI out, MIPI DSI display, eDP display, LVDS display, MIPI CSI camera, TF Card slot, RS485, RS232, TTL, CAN, Power out, SATA, etc.

Android 11, Ubuntu 18.04 OS, Debian OS and Linux Buildroot are supported. The stable and reliable operation provides a safe and stable system environment for product research and production.

A complete SDK, development documents, examples, technology documents, tutorials and other resources are provided for the users to make a further customization.

TC-RK3568 Stamp Hole Development Board Features:

- Size: 150mm x 110mm.
- Rich interfaces, can be directly used in various intelligent products to facilitate the completion of products.
- Android 11.0, Ubuntu 18.04 OS, Debian OS and Linux Buildroot are supported.

1.2 Application

This board can be widely used in smart NVRs, cloud terminals, IoT gateways, industrial control, edge computing, face recognition gates, NASs, vehicle center consoles, etc.

1.3 Characteristic Parameter

Specifications	
CPU	RockChip RK3568, Quad-core 64-bit Cortex-A55, 22nm lithography process, frequency up to 2.0GHz
GPU	ARM G52 2EE Supports OpenGL ES 1.1/2.0/3.2, OpenCL 2.0, Vulkan 1.1 Embedded high-performance 2D acceleration hardware
NPU	0.8Tops@INT8, integrated high-performance AI accelerator RKNN NPU Supports one-click switching of Caffe/TensorFlow/TFLite/ONNX/PyTorch/Keras/Darknet

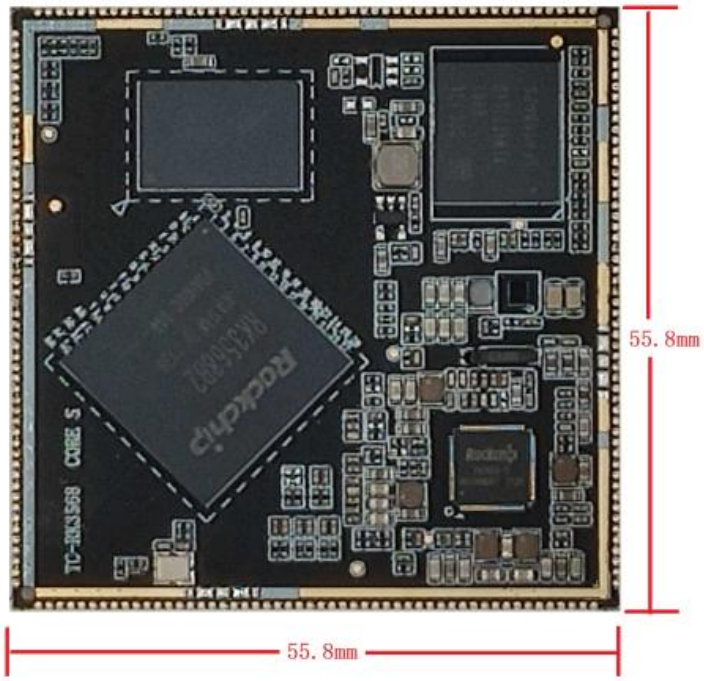
VPU	Supports 4K 60fps H.265/H.264/VP9 video decoding Supports 1080P 100fps H.265/H.264 video encoding Supports 8M ISP, supports HDR
RAM	2GB/4GB/8GB LPDDR4
Storage	8GB/16GB/32GB/64GB/128GB eMMC Supports SATA 3.0 x 1 (Expand with 2.5” SSD/HDD) Supports TF-Card Slot x1 (Expand with TF card)
System OS	Android11/Linux Buildroot/Ubuntu/Debian

Hardware Features	
Display	1 * HDMI2.0, supports 4K@60fps output 1 * MIPI DSI, supports 1920*1080@60fps output 1 * LVDS, supports 1920*1080@60fps output 1 * eDP1.3 , supports 2560x1600@60fps output or 1 * VGA, supports 1920*1080@60fps output
Ethernet	Supports dual Gigabit Ethernet ports(1000 Mbps)
Wifi	Mini PCIe to connect 4G LTE Supports WiFi 6 (802.11 AX) Supports BT5.0
PCIE3.0	Supports PCE3.0 interface
Audio	1 * HDMI audio output 1 * Speaker output 1 * Earphone output 1 * Microphone onboard audio input
Camera	Supports 1-channel MIPI-CSI camera interface Supports HDR, image remains clear under backlight or strong light conditions
USB	1 * USB3.0 Host, 4* USB 2.0 Host, 1 * USB3.0 OTG
SATA	1 * SATA, 6.0Gb/s
Serial	1 * TTL, 2 * RS232, 1 * RS485
CAN	Support CAN2.0B, Support 1Mbps, 8Mbps
TF Card	1 * TF Card Slot

Others	GPIO And ADC
Size	150mm*110mm

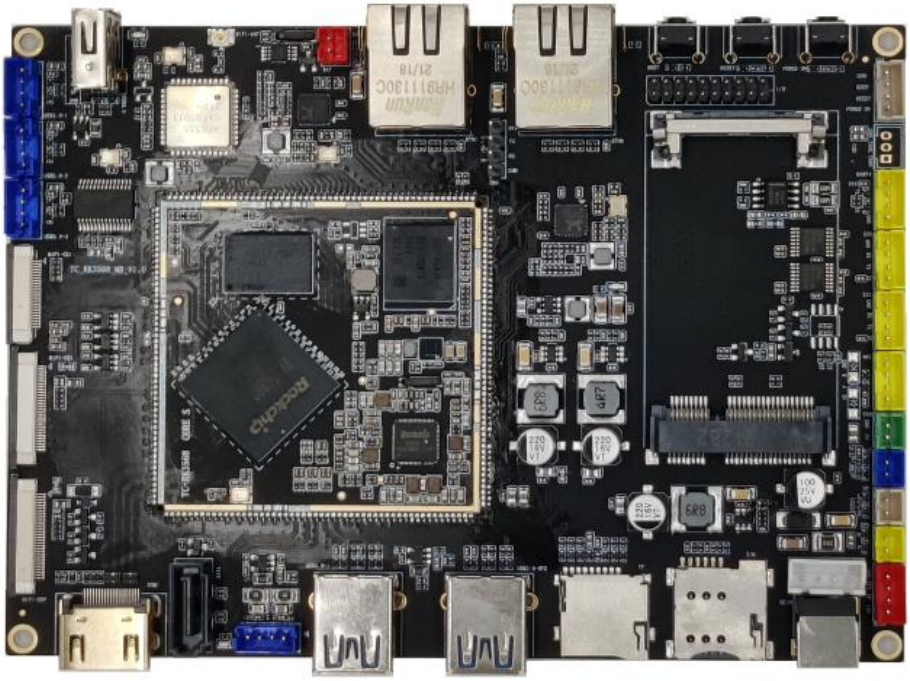
Electrical Specification	
Input Voltage	12V/3A
Storage Temperature	-30~80℃
Operating Temperature	-20~60 ℃
Storage Humidity	10%~80%

1.4 SOM Appearance



SOM Front

1.5 Development Board Appearance



Chapter 2. SOM PIN Definition

2.1 SOM PIN Definition

PIN	Core board pin definition	Default function	Default function description	IO Power Domain	Pad type IO pull
1	VCC3V3_SYS	3.3V System Power Supply	Input Voltage 3.3V		-
2	VCC3V3_SYS	3.3V System Power Supply	Input Voltage 3.3V		-
3	GND	GND	GND		-
4	GND	GND	GND		-
5	SDMMC0_DET_L	SDMMC0_DET/SATA_CP_DET/PCIE30X1_CLKREQn_M0/GPIO0_A4_u	SDMMC0 detect input	3.3V	I/O UP
6	SDMMC0_D3	SDMMC0_D3/ARMJTAG_TMS/UART5_RTSn_M0/GPIO2_A0_u	SDMMC0 data port	3.3V	I/O UP
7	SDMMC0_D2	SDMMC0_D2/ARMJTAG_TCK/UART5_CTSn_M0/GPIO1_D7_u	SDMMC0 data port	3.3V	I/O UP
8	SDMMC0_D1	SDMMC0_D1/UART2_RX_M1/UART6_RX_M1/PWM9_M1/GPIO1_D6_u	SDMMC0 data port	3.3V	I/O UP
9	SDMMC0_D0	SDMMC0_D0/UART2_TX_M1/UART6_TX_M1/PWM8_M1/GPIO1_D5_u	SDMMC0 data port	3.3V	I/O UP
10	SDMMC0_CMD	SDMMC0_CMD/PWM10_M1/UART5_RX_M0/CAN0_TX_M1/GPIO2_A1_u	SDMMC0 command output	3.3V	I/O UP
11	SDMMC0_CLK	SDMMC0_CLK/TEST_CLKOUT/UART5_TX_M0/CAN0_RX_M1/GPIO2_A2_d	SDMMC0 clock output	3.3V	I/O DOWN
12	RESETN	NPOR_U	Reset signal detect	3.3V	-
13	RK809_PWRON	Power On	Power on signal input,external connection power key, active low		-
14	RECOVERY	SARADC_VIN0	AD keyboard input	1.8V	-
15	EXT_EN	EXT_EN	PMIC Power enable output,active high		-
16	HPR_OUT	HPR_OUT	Headphone right out	3.3V	-
17	HPL_OUT	HPL_OUT	Headphone left out	3.3V	-
18	SPKP_OUT	SPKP_OUT	Speak out+	5V/0.6W	-
19	SPKN_OUT	SPKN_OUT	Speak out-	5V/0.6W	-
20	MIC1_INN	MIC1_INN/MIC_R	MIC1_INN	3.3V	-
21	MIC1_INP	MIC1_INP/MIC_L	MIC1_INP	3.3V	-
22	HP_DET_L_GPIO3_C2	LCDC_VSYNC/VOP_BT1120_D14/SPI1_MISO_M1/UART5_TX_M1/I2S1_SDO3_M2/	Headphone detect	3.3V	I/O DOWN

		GPIO3_C2_d			
23	SPK_CTL_H_GPIO3_C3	LCDC_DEN/VOP_BT1120_D15/SPI1_CLK_M1/UART5_RX_M1/I2S1_SCLK_RX_M2/GPIO3_C3_d		3.3V	I/O DOWN
24	VCC3V3_SD	3.3V Power Supply	Output Voltage 3.3V For SD Card,Rated output current 2A		-
25	VCC_3V3	3.3V Power Supply	Output Voltage 3.3V,Rated output current 2A		-
26	VCC_1V8	1.8V Power Supply	Output voltage 1.8V,rated output current 2.5A		-
27	PDM_SDI1_M0_ADC	I2S1_SDO3_M0/I2S1_SDI1_M0/PDM_SDI1_M0/PCIE20_PERSTn_M2/GPIO1_B2_d	PDM_SDI1_M0_ADC	3.3V	IO DOWN
28	PDM_SDI2_M0_ADC	I2S1_SDO2_M0/I2S1_SDI2_M0/PDM_SDI2_M0/PCIE20_WAKEn_M2/ACODEC_ADC_SYNC/GPIO1_B1_d	PDM_SDI2_M0_ADC	3.3V	IO DOWN
29	PDM_SDI3_M0_ADC	I2S1_SDO1_M0/I2S1_SDI3_M0/PDM_SDI3_M0/PCIE20_CLKREQn_M2/ACODEC_DAC_DATAR/GPIO1_B0_d	PDM_SDI3_M0_ADC	3.3V	IO DOWN
30	PDM_CLK1_M0_ADC	I2S1_SCLK_RX_M0/UART4_RX_M0/PDM_CLK1_M0/SPDIF_TX_M0/GPIO1_A4_d	PDM_CLK1_M0_ADC	3.3V	IO DOWN
31	GMAC0_TXD0	GMAC0_TXD0/UART1_RX_M0/GPIO2_B3_u	GMAC0 transmit data	1.8V	I/O UP
32	GMAC0_TXD1	GMAC0_TXD1/UART1_TX_M0/GPIO2_B4_u	GMAC0 transmit data	1.8V	I/O UP
33	GMAC0_TXD2	SDMMC1_D3/GMAC0_TXD2/UART7_TX_M0/GPIO2_A6_u	GMAC0 transmit data	1.8V	I/O UP
34	GMAC0_TXD3	SDMMC1_CMD/GMAC0_TXD3/UART9_RX_M0/GPIO2_A7_u	GMAC0 transmit data	1.8V	I/O UP
35	GMAC0_TXEN	GMAC0_TXEN/UART1_RTSn_M0/SPI1_CLK_M0/GPIO2_B5_u	GMAC0 transmit enable	1.8V	I/O UP
36	GMAC0_TXCLK	SDMMC1_CLK/GMAC0_TXCLK/UART9_TX_M0/GPIO2_B0_d	GMAC0 transmit clock	1.8V	I/O DOWN
37	GMAC0_RXD0	GMAC0_RXD0/UART1_CTSn_M0/SPI1_MISO_M0/GPIO2_B6_u	GMAC0 recieve data	1.8v	I/O UP
38	GMAC0_RXD1	I2S2_SCLK_RX_M0/GMAC0_RXD1/UART6_RTSn_M0/SPI1_MOSI_M0/GPIO2_B7_d	GMAC0 recieve data	1.8V	I/O DOWN
39	GMAC0_RXD2	SDMMC1_D0/GMAC0_RXD2/UART6_RX_M0/GPIO2_A3_u	GMAC0 recieve data	1.8v	I/O UP
40	GMAC0_RXD3	SDMMC1_D1/GMAC0_RXD3/UART6_TX_M0/GPIO2_A4_u	GMAC0 recieve data	1.8V	I/O UP

41	GMAC0_RXDV_CRS	I2S2_LRCK_RX_M0/GMAC0_RXDV_CRS/UART6_CTSn_M0/SPI1_CS0_M0/GPIO2_C0_d	GMAC0 RX data valid signal	1.8V	I/O DOWN
42	GMAC0_RXCLK	SDMMC1_D2/GMAC0_RXCLK/UART7_RX_M0/GPIO2_A5_u	GMAC0 receive clock	1.8V	I/O UP
43	ETH0_REFCLKO_25M	I2S2_MCLK_M0/ETH0_REFCLKO_25M/UART7_RTSn_M0/SPI2_CLK_M0/GPIO2_C1_d	ETH0_REF CLOCK OUTPUT_25MHz CPU to PHY,Default NC	1.8V	I/O DOWN
44	GMAC0_MCLKINOUT	I2S2_SCLK_TX_M0/GMAC0_MCLKINOUT/UART7_CTSn_M0/SPI2_MISO_M0/GPIO2_C2_d	GMAC0 external clock input	1.8V	I/O DOWN
45	GMAC0_MDC	I2S2_LRCK_TX_M0/GMAC0_MDC/UART9_RTSn_M0/SPI2_MOSI_M0/GPIO2_C3_d	MAC0 management clock	1.8V	I/O DOWN
46	GMAC0_MDIO	I2S2_SDO_M0/GMAC0_MDIO/UART9_CTSn_M0/SPI2_CS0_M0/GPIO2_C4_d	MAC0 management command and data	1.8V	I/O DOWN
47	GMAC0_RSTN_GPIO3_B7	LCDC_D21/VOP_BT1120_D12/GMAC1_TXD1_M0/I2C3_SDA_M1/PWM11_IR_M0/GPIO3_B6_d		3.3V	IO DOWN
48	GMAC0_INT_PMEB_GPIO3_C0	LCDC_HSYNC/VOP_BT1120_D13/SPI1_MOSI_M1/PCIE20_PERSTn_M1/I2S1_SDO2_M2/GPIO3_C1_d		3.3V	I/O DOWN
49	RTCTC_INT_L_GPIO0_D3	GPIO0_D3_d	RTC_IC_INT,active low	1.8V	I/O DOWN
50	I2C5_SDA_M0	LCDC_D19/VOP_BT1120_D10/GMAC1_RXER_M0/I2C5_SDA_M0/PDM_SDI1_M2/GPIO3_B4_d	I2C serial port 5	3.3V	I/O DOWN
51	I2C5_SCL_M0	LCDC_D18/VOP_BT1120_D9/GMAC1_RXDV_CRS_M0/I2C5_SCL_M0/PDM_SDI0_M2/GPIO3_B3_d	I2C serial port 5	3.3V	I/O DOWN
52	PWM3_IR	PWM3_IR/EDP_HPDIN_M1/PCIE30X1_WAKEn_M0/MCU_JTAG_TMS/GPIO0_C2_d		3.3V	I/O DOWN
53	CAN1_TX_M1	PWM15_IR_M1/SPI3_MOSI_M1/CAN1_TX_M1/PCIE30X2_WAKEn_M2/I2S3_SCLK_M1/GPIO4_C3_d	CAN data transmit	3.3V	I/O DOWN
54	CAN1_RX_M1	PWM14_M1/SPI3_CLK_M1/CAN1_RX_M1/PCIE30X2_CLKREQn_M2/I2S3_MCLK_M1/GPIO4_C2_d	CAN data recieve	3.3V	I/O DOWN
55	UART2_RX_M0_DEBUG	UART2_RX_M0/GPIO0_D0_u	UART serial port data recieve for debug	3.3V	I/O UP
56	UART2_TX_M0_DEBUG	UART2_TX_M0/GPIO0_D1_u	UART serial port data transmit for debug	3.3V	I/O UP
57	UART3_RX_M1	LCDC_D23/PWM13_M0/GMAC1_MCLKINOUT_M0/UART3_RX_M1/PDM_SDI3_M2/GPIO3_C0_d	UART searial port data recieve	3.3V	I/O DOWN

58	UART3_TX_M1	LCDC_D22/PWM12_M0/GMAC1_TXEN_M0/UART3_TX_M1/PDM_SDI2_M2/GPIO3_B7_d	UART searial port data transmit	3.3V	I/O DOWN
59	UART4_TX_M1	LCDC_D17/VOP_BT1120_D8/GMAC1_RXD1_M0/UART4_TX_M1/PWM9_M0/GPIO3_B2_d	UART searial port data transmit	3.3V	I/O DOWN
60	UART4_RX_M1	LCDC_D16/VOP_BT1120_D7/GMAC1_RXD0_M0/UART4_RX_M1/PWM8_M0/GPIO3_B1_d	UART searial port data recieve	3.3V	I/O DOWN
61	UART9_RX_M1	PWM13_M1/SPI3_CS0_M1/SATA0_ACT_LED/UART9_RX_M1/I2S3_SDI_M1/GPIO4_C6_d	UART searial port data recieve	3.3V	I/O DOWN
62	UART9_TX_M1	PWM12_M1/SPI3_MISO_M1/SATA1_ACT_LED/UART9_TX_M1/I2S3_SDO_M1/GPIO4_C5_d	UART searial port data transmit	3.3V	I/O DOWN
63	UART7_RX_M1	PWM15_IR_M0/SPDIF_TX_M1/GMAC1_MDIO_M0/UART7_RX_M1/I2S1_LRCK_RX_M2/GPIO3_C5_d	UART searial port data recieve	3.3V	I/O DOWN
64	UART7_TX_M1	PWM14_M0/VOP_PWM_M1/GMAC1_MDC_M0/UART7_TX_M1/PDM_CLK1_M2/GPIO3_C4_d	UART searial port data transmit	3.3V	I/O DOWN
65	RS485_DIR_GPIO3_B5	LCDC_D20/VOP_BT1120_D11/GMAC1_TXD0_M0/I2C3_SCL_M1/PWM10_M0/GPIO3_B5_d	RS485 data direction	3.3V	I/O DOWN
66	DVP_PWREN0_H_GPIO0_B0	CLK32K_IN/CLK32K_OUT0/PCIE30X2_BUTTONRSTn/GPIO0_B0_u		3.3V	I/O UP
67	WIFI_PWREN_L_GPIO0_C1	PWM2_M0/NPUAVS/UART0_TX/MCU_JTAG_TDI/GPIO0_C1_d		3.3V	I/O DOWN
68	I2S3_SDI_M0	LCDC_D13/VOP_BT1120_CLK/GMAC1_TXCLK_M0/I2S3_SDI_M0/SDMMC2_CLK_M1/GPIO3_A6_d	I2S3_SDI	3.3V	I/O DOWN
69	I2S3_SDO_M0	LCDC_D12/VOP_BT1120_D4/GMAC1_RXD3_M0/I2S3_SDO_M0/SDMMC2_CMD_M1/GPIO3_A5_d	I2S3_SDO	3.3V	I/O DOWN
70	I2S3_LRCK_M0	LCDC_D11/VOP_BT1120_D3/GMAC1_RXD2_M0/I2S3_LRCK_M0/SDMMC2_D3_M1/GPIO3_A4_d	I2S3_LRCK	3.3V	I/O DOWN
71	I2S3_SCLK_M0	LCDC_D10/VOP_BT1120_D2/GMAC1_TXD3_M0/I2S3_SCLK_M0/SDMMC2_D2_M1/GPIO3_A3_d	I2S3_SCLK	3.3V	I/O DOWN
72	HOST_WAKE_BT_H_GPIO3_A2	LCDC_D9/VOP_BT1120_D1/GMAC1_TXD2_M0/I2S3_MCLK_M0/SDMMC2_D1_M1/GPIO3_A2_d	HOST_WAKE_BT	3.3V	I/O DOWN
73	BT_WAKE_HOST_H_GPIO3_A1	LCDC_D8/VOP_BT1120_D0/SPI1_CS0_M1/PCIE30X1_PERSTn_M1/SDMMC2_D0_M1/GPIO3_A1_d	BT_WAKE_HOST	3.3V	I/O DOWN

74	BT_REG_ON_H_GPIO3_A0	LCDC_CLK/VOP_BT656_CLK_M0/SPI2_CLK_M1/UART8_RX_M1/I2S1_SDO1_M2/GPIO3_A0_d	Bluetooth module power enable	3.3V	I/O DOWN
75	UART8_RX_M0	CLK32K_OUT1/UART8_RX_M0/SPI1_CS1_M0/GPIO2_C6_d	UART searial port data recieve	1,8V	I/O DOWN
76	UART8_TX_M0	I2S2_SDI_M0/GMAC0_RXER/UART8_TX_M0/SPI2_CS1_M0/GPIO2_C5_d	UART searial port data transmit	1.8V	I/O DOWN
77	UART8_CTSN_M0	SDMMC1_DET/I2C4_SCL_M1/UART8_CTSn_M0/CAN2_TX_M1/GPIO2_B2_u	UART8_CTSn_M0	1.8V	I/O DOWN
78	UART8_RTSN_M0	SDMMC1_PWREN/I2C4_SDA_M1/UART8_RTSn_M0/CAN2_RX_M1/GPIO2_B1_d	UART8_RTSn_M0	1.8V	I/O DOWN
79	WIFI_REG_ON_H_GPIO3_D5	CIF_D7/EBC_SDDO7/SDMMC2_PWREN_M0/I2S1_SDI3_M1/VOP_BT656_D7_M1/GPIO3_D5_d	WIFI_REG enable	1.8V	I/O DOWN
80	WIFI_WAKE_HOST_H_GPIO3_D4	CIF_D6/EBC_SDDO6/SDMMC2_DET_M0/I2S1_SDI2_M1/VOP_BT656_D6_M1/GPIO3_D4_d	WIFI wake up host	1.8V	I/O DOWN
81	SDMMC2_CLK_M0	CIF_D5/EBC_SDDO5/SDMMC2_CLK_M0/I2S1_SDI1_M1/VOP_BT656_D5_M1/GPIO3_D3_d	SDMMC2 clock	1.8V	I/O DOWN
82	SDMMC2_CMD_M0	CIF_D4/EBC_SDDO4/SDMMC2_CMD_M0/I2S1_SDI0_M1/VOP_BT656_D4_M1/GPIO3_D2_d	SDMMC2 command	1.8V	I/O DOWN
83	SDMMC2_D3_M0	CIF_D3/EBC_SDDO3/SDMMC2_D3_M0/I2S1_SDO0_M1/VOP_BT656_D3_M1/GPIO3_D1_d	SDMMC2 data	1.8V	I/O DOWN
84	SDMMC2_D2_M0	CIF_D2/EBC_SDDO2/SDMMC2_D2_M0/I2S1_LRCK_TX_M1/VOP_BT656_D2_M1/GPIO3_D0_d	SDMMC2 data	1.8V	I/O DOWN
85	SDMMC2_D1_M0	CIF_D1/EBC_SDDO1/SDMMC2_D1_M0/I2S1_SCLK_TX_M1/VOP_BT656_D1_M1/GPIO3_C7_d	SDMMC2 data	1.8V	I/O DOWN
86	SDMMC2_D0_M0	CIF_D0/EBC_SDDO0/SDMMC2_D0_M0/I2S1_MCLK_M1/VOP_BT656_D0_M1/GPIO3_C6_d	SDMMC2 data	1.8V	I/O DOWN
87	GMAC1_INT/PMEB_GPIO3_A7	LCDC_D14/VOP_BT1120_D5/GMAC1_RXCLK_M0/SDMMC2_DET_M1/GPIO3_A7_d		3.3V	I/O DOWN
88	GMAC1_RSTN_GPIO3_B0	LCDC_D15/VOP_BT1120_D6/ETH1_REFCLKO_25M_M0/SDMMC2_PWREN_M1/GPIO3_B0_d		3.3V	I/O DOWN
89	GMAC1_MDIO_M1	IF_VSYNC/EBC_SDOE/GMAC1_MDIO_M1/I2S2_SCLK_TX_M1/GPIO4_B7_d	GMAC1 management command and data	1.8V	I/O DOWN
90	GMAC1_MDC_M1	CIF_HREF/EBC_SDLE/GMAC1_MDC_M1/UART1_RTS	GMAC1 management clock	1.8V	I/O DOWN

		n_M1/I2S2_MCLK_M1/GPIO4_B6_d			
91	GMAC1_MCLKINOUT_M1	CIF_CLKIN/EBC_SDCLK/GMAC1_MCLKINOUT_M1/UART1_CTSn_M1/I2S2_SCLK_RX_M1/GPIO4_C1_d	GMAC1 external clock input	1.8V	I/O DOWN
92	ETH1_REFCLKO_25M_M1	I2C4_SCL_M0/EBC_GDOE/ETH1_REFCLKO_25M_M1/SPI3_CLK_M0/I2S2_SDO_M1/GPIO4_B3_d	ETH1 Clock output	1.8V	I/O DOWN
93	GMAC1_RXCLK_M1	CIF_D13/EBC_SDDO13/GMAC1_RXCLK_M1/UART7_RX_M2/PDM_SDI3_M1/GPIO4_A3_d	GMAC1 receive clock	1.8V	I/O DOWN
94	GMAC1_RXDV_CRS_M1	ISP_PRELIGHT_TRIG/EBC_SDCE3/GMAC1_RXDV_CRS_M1/I2S1_SDO2_M1/GPIO4_B1_d	GMAC1 RX data valid signal	1.8V	I/O DOWN
95	GMAC1_RXD3_M1	CIF_D12/EBC_SDDO12/GMAC1_RXD3_M1/UART7_TX_M2/PDM_SDI2_M1/GPIO4_A2_d	GMAC1 recieve data	1.8V	I/O DOWN
96	GMAC1_RXD2_M1	CIF_D11/EBC_SDDO11/GMAC1_RXD2_M1/PDM_SDI1_M1/GPIO4_A1_d	GMAC1 recieve data	1.8V	I/O DOWN
97	GMAC1_RXD1_M1	CAM_CLKOUT1/EBC_SDCE2/GMAC1_RXD1_M1/SPI3_MISO_M0/I2S1_SDO1_M1/GPIO4_B0_d	GMAC1 recieve data	1.8V	I/O DOWN
98	GMAC1_RXD0_M1	CAM_CLKOUT0/EBC_SDCE1/GMAC1_RXD0_M1/SPI3_CS1_M0/I2S1_LRCK_RX_M1/GPIO4_A7_d	GMAC1 recieve data	1.8V	I/O DOWN
99	GMAC1_TXCLK_M1	CIF_D10/EBC_SDDO10/GMAC1_TXCLK_M1/PDM_CLK1_M1/GPIO4_A0_d	GMAC1 transmit clock	1.8V	I/O DOWN
100	GMAC1_TXEN_M1	ISP_FLASHTRIGOUT/EBC_SDCE0/GMAC1_TXEN_M1/SPI3_CS0_M0/I2S1_SCLK_RX_M1/GPIO4_A6_d	GMAC1 transmit enable	1.8V	I/O DOWN
101	GMAC1_TXD3_M1	CIF_D9/EBC_SDDO9/GMAC1_TXD3_M1/UART1_RX_M1/PDM_SDI0_M1/GPIO3_D7_d	GMAC1 transmit data	1.8V	I/O DOWN
102	GMAC1_TXD2_M1	CIF_D8/EBC_SDDO8/GMAC1_TXD2_M1/UART1_TX_M1/PDM_CLK0_M1/GPIO3_D6_d	GMAC1 transmit data	1.8V	I/O DOWN
103	GMAC1_TXD1_M1	CIF_D15/EBC_SDDO15/GMAC1_TXD1_M1/UART9_RX_M2/I2S2_LRCK_RX_M1/GPIO4_A5_d	GMAC1 transmit data	1.8V	I/O DOWN
104	GMAC1_TXD0_M1	CIF_D14/EBC_SDDO14/GMAC1_TXD0_M1/UART9_TX_M2/I2S2_LRCK_TX_M1/GPIO4_A4_d	GMAC1 transmit data	1.8V	I/O DOWN
105	TP_RST_L_GPIO0_B6	I2C2_SDA_M0/SPI0_MOSI_M0/PCIE20_PERSTn_M0/PWM2_M1/GPIO0_B6_u	Touchpanel reset	3.3V	I/O UP
106	TP_INT_L_GPIO0_B5	I2C2_SCL_M0/SPI0_CLK_	Touchpanel interrupt data	3.3V	I/O UP

		M0/PCIE20_WAKEn_M0/PWM1_M1/GPIO0_B5_u	input		
107	I2C1_SDA_TP	I2C1_SDA/CAN0_RX_M0/PCIE20_BUTTONRSTn/MCU_JTAG_TCK/GPIO0_B4_u	I2C serial port 1	3.3V	I/O UP
108	I2C1_SCL_TP	I2C1_SCL/CAN0_TX_M0/PCIE30X1_BUTTONRSTn/MCU_JTAG_TDO/GPIO0_B3_u	I2C serial port 1	3.3V	I/O UP
109	I2C3_SCL_M0	I2C3_SCL_M0/UART3_TX_M0/CAN1_TX_M0/AUDIOPWM_LOUT_N/ACODEC_ADC_CLK/GPIO1_A1_u	I2C serial port 3	3.3V	I/O UP
110	I2C3_SDA_M0	I2C3_SDA_M0/UART3_RX_M0/CAN1_RX_M0/AUDIOPWM_LOUT_P/ACODEC_ADC_DATA/GPIO1_A0_u	I2C serial port 3	3.3V	I/O UP
111	I2C2_SCL_M1	I2C2_SCL_M1/EBC_SDSHR/CAN2_TX_M0/I2S1_SDO3_M1/GPIO4_B5_d	I2C serial port 2	1.8V	I/O DOWN
112	I2C2_SDA_M1	I2C2_SDA_M1/EBC_GDSP/CAN2_RX_M0/ISP_FLASH_TRIGIN/VOP_BT656_CLK_M1/GPIO4_B4_d	I2C serial port 2	1.8V	I/O DOWN
113	MIPI_CAM1_PDN_L_GPIO3_D3	LCDC_D1/VOP_BT656_D1_M0/SPI0_MOSI_M1/PCIE20_WAKEn_M1/I2S1_SCLK_TX_M2/GPIO2_D1_d	Camera1 power down	3.3V	I/O DOWN
114	MIPI_CAM1_RST_L_GPIO3_D2	LCDC_D0/VOP_BT656_D0_M0/SPI0_MISO_M1/PCIE20_CLKREQn_M1/I2S1_MCLK_M2/GPIO2_D0_d	Camera1 reset	3.3V	I/O DOWN
115	MIPI_CAM0_RST_L_GPIO3_D4	LCDC_D2/VOP_BT656_D2_M0/SPI0_CS0_M1/PCIE30X1_CLKREQn_M1/I2S1_LRCK_TX_M2/GPIO2_D2_d	Camera0 reset	3.3V	I/O DOWN
116	MIPI_CAM0_PDN_L_GPIO3_D5	LCDC_D3/VOP_BT656_D3_M0/SPI0_CLK_M1/PCIE30X1_WAKEn_M1/I2S1_SDI0_M2/GPIO2_D3_d	Camera0 power down	3.3V	I/O DOWN
117	USB2_HOST2_DM	USB2_HOST2_DM	USB2_HOST2_DM	3.3V	-
118	USB2_HOST2_DP	USB2_HOST2_DP	USB2_HOST2_DP	3.3V	-
119	USB2_HOST3_DM	USB2_HOST3_DM	USB2_HOST3_DM	3.3V	-
120	USB2_HOST3_DP	USB2_HOST3_DP	USB2_HOST3_DP	3.3V	-
121	REFCLK_OUT	REFCLK_OUT/GPIO0_A0_d	Clock output for camera	3.3V	I/O DOWN
122	CIF_CLKOUT	CIF_CLKOUT/EBC_GDCLK/PWM11_IR_M1/GPIO4_C0_d	CIF clock out	1.8V	I/O DOWN
123	MIPI_CSI_RX_D3P	MIPI_CSI_RX_D3P	MIPI_CSI_RX_D3P	1.8V	-
124	MIPI_CSI_RX_D3N	MIPI_CSI_RX_D3N	MIPI_CSI_RX_D3N	1.8V	-
125	MIPI_CSI_RX_D2P	MIPI_CSI_RX_D2P	MIPI_CSI_RX_D2P	1.8V	-
126	MIPI_CSI_RX_D2N	MIPI_CSI_RX_D2N	MIPI_CSI_RX_D2N	1.8V	-

127	MIPI_CSI_RX_CLK1P	MIPI_CSI_RX_CLK1P	MIPI_CSI_RX_CLK1P	1.8V	-
128	MIPI_CSI_RX_CLK1N	MIPI_CSI_RX_CLK1N	MIPI_CSI_RX_CLK1N	1.8V	-
129	MIPI_CSI_RX_CLK0P	MIPI_CSI_RX_CLK0P	MIPI_CSI_RX_CLK0P	1.8V	-
130	MIPI_CSI_RX_CLK0N	MIPI_CSI_RX_CLK0N	MIPI_CSI_RX_CLK0N	1.8V	-
131	MIPI_CSI_RX_D1P	MIPI_CSI_RX_D1P	MIPI_CSI_RX_D1P	1.8V	-
132	MIPI_CSI_RX_D1N	MIPI_CSI_RX_D1N	MIPI_CSI_RX_D1N	1.8V	-
133	MIPI_CSI_RX_D0P	MIPI_CSI_RX_D0P	MIPI_CSI_RX_D0P	1.8V	-
134	MIPI_CSI_RX_D0N	MIPI_CSI_RX_D0N	MIPI_CSI_RX_D0N	1.8V	-
135	LCD1_PWREN_H_GPIO0_C5	PWM6/SPI0_MISO_M0/PCIE30X2_WAKEn_M0/GPIO0_C5_d	LCD power enable	3.3V	I/O DOWN
136	LCD1_BL_PWM5	PWM5/SPI0_CS1_M0/UART0_RTSn/GPIO0_C4_d	LCD backlight PWM	3.3V	I/O DOWN
137	LCD1_BL_PWM4	PWM4/VOP_PWM_M0/PCIE30X1_PERSTn_M0/MCU_JTAG_TRSTn/GPIO0_C3_d	LCD backlight PWM	3.3V	I/O DOWN
138	LCD0_PWREN_H_GPIO0_C7	HDMITX_CEC_M1/PWM0_M1/UART0_CTSn/GPIO0_C7_d	LCD power enable	3.3V	I/O DOWN
139	MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	1.8V	-
140	MIPI_DSI_TX0_D3P/LVDS_TX0_D3N	MIPI_DSI_TX0_D3P/LVDS_TX0_D3N	MIPI_DSI_TX0_D3P/LVDS_TX0_D3N	1.8V	-
141	MIPI_DSI_TX0_D3P/LVDS_TX0_D2P	MIPI_DSI_TX0_D3P/LVDS_TX0_D2P	MIPI_DSI_TX0_D3P/LVDS_TX0_D2P	1.8V	-
142	MIPI_DSI_TX0_D3P/LVDS_TX0_D2N	MIPI_DSI_TX0_D3P/LVDS_TX0_D2N	MIPI_DSI_TX0_D3P/LVDS_TX0_D2N	1.8V	-
143	MIPI_DSI_TX0_D3P/LVDS_TX0_CLKP	MIPI_DSI_TX0_D3P/LVDS_TX0_CLKP	MIPI_DSI_TX0_D3P/LVDS_TX0_CLKP	1.8V	-
144	MIPI_DSI_TX0_D3P/LVDS_TX0_CLKN	MIPI_DSI_TX0_D3P/LVDS_TX0_CLKN	MIPI_DSI_TX0_D3P/LVDS_TX0_CLKN	1.8V	-
145	MIPI_DSI_TX0_D3P/LVDS_TX0_D1P	MIPI_DSI_TX0_D3P/LVDS_TX0_D1P	MIPI_DSI_TX0_D3P/LVDS_TX0_D1P	1.8V	-
146	MIPI_DSI_TX0_D3P/LVDS_TX0_D1N	MIPI_DSI_TX0_D3P/LVDS_TX0_D1N	MIPI_DSI_TX0_D3P/LVDS_TX0_D1N	1.8V	-
147	MIPI_DSI_TX0_D3P/LVDS_TX0_D0P	MIPI_DSI_TX0_D3P/LVDS_TX0_D0P	MIPI_DSI_TX0_D3P/LVDS_TX0_D0P	1.8V	-
148	MIPI_DSI_TX0_D3P/LVDS_TX0_D0N	MIPI_DSI_TX0_D3P/LVDS_TX0_D0N	MIPI_DSI_TX0_D3P/LVDS_TX0_D0N	1.8V	-
149	HDMI_TXCLKN_PORT	HDMI_TX_CLKN	HDMI_TX2CLKN_PORT,and series resistance 2.2R	1.8V	-
150	HDMI_TXCLKP_PORT	HDMI_TX_CLKP	HDMI_TXCLKP_PORT,and series resistance 2.2R	1.8V	-
151	HDMI_TX0N_PORT	HDMI_TX_D0N	HDMI_TX0N_PORT,and series resistance 2.2R	1.8V	-
152	HDMI_TX0P_PORT	HDMI_TX_D0P	HDMI_TX0P_PORT,and series resistance 2.2R	1.8V	-

153	HDMI_TX1N_PORT	HDMI_TX_D1N	HDMI_TX1N_PORT,and series resistance 2.2R	1.8V	-
154	HDMI_TX1P_PORT	HDMI_TX_D1P	HDMI_TX1P_PORT,and series resistance 2.2R	1.8V	-
155	HDMI_TX2N_PORT	HDMI_TX_D2N	HDMI_TX2N_PORT,and series resistance 2.2R	1.8V	-
156	HDMI_TX2P_PORT	HDMI_TX_D2P	HDMI_TX2P_PORT,and series resistance 2.2R	1.8V	-
157	HDMITX_SCL	HDMITX_SCL/I2C5_SCL_M1/GPIO4_C7_u	I2C serial port for HDMI	3.3V	I/O UP
158	HDMITC_SDA	HDMITX_SDA/I2C5_SDA_M1/GPIO4_D0_u	I2C serial port for HDMI	3.3V	I/O UP
159	HDMITX_CEC_M0	HDMITX_CEC_M0/SPI3_CS1_M1/GPIO4_D1_u	HDMITX_CEC	3.3V	I/O UP
160	HDMI_TX_HPDIN	HDMI_TX_HPDIN	HDMI_TX hot plug	1.8V	-
161	PCIE30X2_CLKREQN_M1	LCDC_D4/VOP_BT656_D4_M0/SPI2_CS1_M1/PCIE30X2_CLKREQn_M1/I2S1_SDI1_M2/GPIO2_D4_d	PCIE30X2_CLKREQn	3.3	I/O DOWN
162	PCIE30X2_WAKEN_M1	LCDC_D5/VOP_BT656_D5_M0/SPI2_CS0_M1/PCIE30X2_WAKEn_M1/I2S1_SDI2_M2/GPIO2_D5_d	PCIE30X2_WAKEn	3.3V	I/O DOWN
163	PCIE30X2_PERSTN_M1	LCDC_D6/VOP_BT656_D6_M0/SPI2_MOSI_M1/PCIE30X2_PERSTn_M1/I2S1_SDI3_M2/GPIO2_D6_d	PCIE30X2 reset	3.3V	I/O DOWN
164	PCIE30X2_PRSNT_L_GPIO2_D7	LCDC_D7/VOP_BT656_D7_M0/SPI2_MISO_M1/UART8_TX_M1/I2S1_SDO0_M2/GPIO2_D7_d	PCIE30X2 wake host	3.3V	I/O DOWN
165	PCIE_PWREN_H_GPIO0_D4	GPIO0_D4_d	PCIE power enable	1.8V	I/O DOWN
166	PCIE30_RX1N	PCIE30_RX1N	PCIE30_RX1N	1.8V	-
167	PCIE30_RX1P	PCIE30_RX1P	PCIE30_RX1P	1.8V	-
168	PCIE30_RX0N	PCIE30_RX0N	PCIE30_RX0N	1.8V	-
169	PCIE30_RX0P	PCIE30_RX0P	PCIE30_RX0P	1.8V	-
170	PCIE30_TX1N	PCIE30_TX1N	PCIE30_TX1N	1.8V	-
171	PCIE30_TX1P	PCIE30_TX1P	PCIE30_TX1P	1.8V	-
172	PCIE30_TX0N	PCIE30_TX0N	PCIE30_TX0N	1.8V	-
173	PCIE30_TX0P	PCIE30_TX0P	PCIE30_TX0P	1.8V	-
174	PCIE30_REFCLKN_IN	PCIE30_REFCLKN_IN	PCIE30_REFCLKN_IN	1.8V	-
175	PCIE30_REFCLKP_IN	PCIE30_REFCLKP_IN	PCIE30_REFCLKP_IN	1.8V	-
176	PCIE20_REFCLKN	PCIE20_REFCLKN	PCIE20_REFCLKN	1.8V	-
177	PCIE20_REFCLKP	PCIE20_REFCLKP	PCIE20_REFCLKP	1.8V	-
178	SATA2_RXN	PCIE20_RXN/SATA2_RXN/QSGMII_RXN_M1	SATA2_RXN	1.8V	-

179	SATA2_RXP	PCIE20_RXP/SATA2_RXP/QSGMII_RXP_M1	SATA2_RXP	1.8V	-
180	SATA2_TXN	PCIE20_TXN/SATA2_TXN/QSGMII_TXN_M1	SATA2_TXN	1.8V	-
181	SATA2_TXP	PCIE20_TXP/SATA2_TXP/QSGMII_TXP_M1	SATA2_TXP	1.8V	-
182	SATA2_ACT_LED	EDP_HPDIN_M0/SPDIF_TX_M2/SATA2_ACT_LED/PCIE30X2_PERSTn_M2/I2S3_LRCK_M1/GPIO4_C4_d	SATA active indicate	3.3V	I/O DOWN
183	USB3_HOST1_SSTXP	USB3_HOST1_SSTXP/SATA1_TXP/QSGMII_TXP_M0	USB3_HOST1_SSTXP	1.8V	-
184	USB3_HOST1_SSTXN	USB3_HOST1_SSTXN/SATA1_TXN/QSGMII_TXN_M0	USB3_HOST1_SSTXN	1.8V	-
185	USB3_HOST1_SSRXP	USB3_HOST1_SSRXP/SATA1_RXP/QSGMII_RXP_M0	USB3_HOST1_SSRXP	1.8V	-
186	USB3_HOST1_SSRXN	USB3_HOST1_SSRXN/SATA1_RXN/QSGMII_RXN_M0	USB3_HOST1_SSRXN	1.8V	-
187	USB3_HOST1_DM	USB3_HOST1_DM	USB3_HOST1_DM	3.3V	-
188	USB3_HOST1_DP	USB3_HOST1_DP	USB3_HOST1_DP	3.3V	-
189	USB3_OTG0_SSTXP	USB3_OTG0_SSTXP/SATA0_TXP	USB3_OTG0_SSTXP	1.8V	-
190	USB3_OTG0_SSTXN	USB3_OTG0_SSTXN/SATA0_TXN	USB3_OTG0_SSTXN	1.8V	-
191	USB3_OTG0_SSRXP	USB3_OTG0_SSRXP/SATA0_RXP	USB3_OTG0_SSRXP	1.8V	-
192	USB3_OTG0_SSRXN	USB3_OTG0_SSRXN/SATA0_RXN	USB3_OTG0_SSRXN	1.8V	-
193	USB3_OTG0_DM	USB3_OTG0_DM	USB3_OTG0_DM	3.3V	-
194	USB3_OTG0_DP	USB3_OTG0_DP	USB3_OTG0_DP	3.3V	-
195	USB3_OTG0_ID	USB3_OTG0_ID	USB3_OTG0_ID	3.3V	-
196	USB3_OTG0_VBUSDET	USB3_OTG0_VBUSDET	USB3_OTG0_VBUS detect	3.3V	-
197	USB_HOST_PWREN_H_GPIO0_A6	GPU_PWREN/SATA_CP_POD/PCIE30X2_CLKREQn_M0/GPIO0_A6_d	USB host power enable	3.3V	I/O DOWN
198	USB_OTG_PWREN_H_GPIO0_A5	SDMMC0_PWREN/SATA_MP_SWITCH/PCIE20_CLKREQn_M0/GPIO0_A5_d	USB OTG power enable	3.3V	I/O DOWN
199	DSI_TX1_D3N/EDP_TX_D3N	MIPI_DSI_TX1_D3N/EDP_TX_D3N	MIPI_DSI_TX1_D3N/EDP_TX_D3N	1.8V	-
200	DSI_TX1_D3P/EDP_TX_D3P	MIPI_DSI_TX1_D3P/EDP_TX_D3P	MIPI_DSI_TX1_D3P/EDP_TX_D3P	1.8V	-
201	DSI_TX1_D2N/EDP_TX_D2N	MIPI_DSI_TX1_D2N/EDP_TX_D2N	MIPI_DSI_TX1_D2N/EDP_TX_D2N	1.8V	-
202	DSI_TX1_D2P/EDP_TX_D2P	MIPI_DSI_TX1_D2P/EDP_TX_D2P	MIPI_DSI_TX1_D2P/EDP_TX_D2P	1.8v	-
203	DSI_TX1_D1N/EDP_TX_D1N	MIPI_DSI_TX1_D1N/EDP_TX_D1N	MIPI_DSI_TX1_D1N/EDP_TX_D1N	1.8V	-

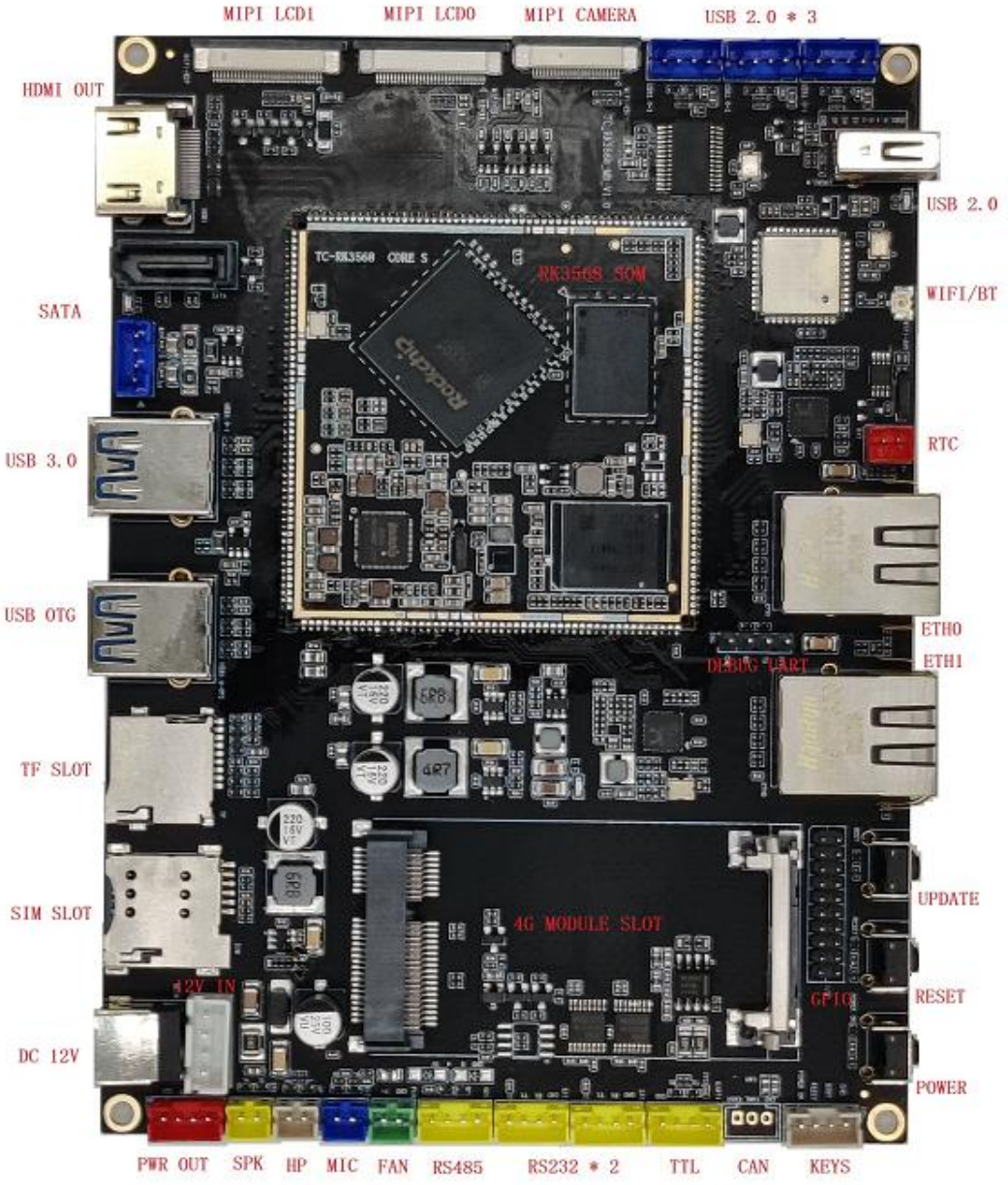
204	DSI_TX1_D1P/EDP_TX_D1P	MIPI_DSI_TX1_D1P/EDP_TX_D1P	MIPI_DSI_TX1_D1P/EDP_TX_D1P	1.8V	-
205	DSI_TX1_D0N/EDP_TX_D0N	MIPI_DSI_TX1_D0N/EDP_TX_D0N	MIPI_DSI_TX1_D0N/EDP_TX_D0N	1.8V	-
206	DSI_TX1_D0P/EDP_TX_D0P	MIPI_DSI_TX1_D0P/EDP_TX_D0P	MIPI_DSI_TX1_D0P/EDP_TX_D0P	1.8V	-
207	DSI_TX1_CLKN/EDP_TX_AUN	MIPI_DSI_TX1_CLKN/EDP_TX_AUN	MIPI_DSI_TX1_CLKN/EDP_TX_AUN	1.8V	-
208	DSI_TX1_CLKP/EDP_TX_AUP	MIPI_DSI_TX1_CLKP/EDP_TX_AUP	MIPI_DSI_TX1_CLKP/EDP_TX_AUP	1.8V	-

Chapter 3. Development Board

3.1 Size

The size is 150mm*110mm, 4 layers, 1.6mm thickness .

3.2 Interfaces Description



Interfaces Description	
NO.#	Name
【1】	DC 12V Input/4pin 2.54mm 12V Input

【2】	4G module sim card slot
【3】	TF card slot
【4】	USB OTG
【5】	USB3.0 HOST
【6】	SATA Data & Power
【7】	HDMI Out
【8】	MIPI LCD1
【9】	MIPI LCD0
【10】	MIPI Camera
【11】	USB2.0 * 3
【12】	USB2.0 TypeA
【13】	WIFI/BT(AP6335)
【14】	RTC
【15】	ETH0
【16】	ETH1
【17】	Update Key
【18】	Reset Key
【19】	Power Key
【20】	Keys(4pin 2.0mm)
【21】	CAN(3pin 2.0mm)
【22】	Uart TTL(4pin 2.0mm)
【23】	RS232 * 2(4pin 2.0mm)
【24】	RS485(4pin 2.0mm)
【25】	FAN(2pin 2.0mm)
【26】	MIC(2pin 2.0mm)
【27】	HP(2pin 2.0mm)
【28】	SPK(2pin 2.0mm)
【29】	Power Out(4pin 2.0mm)
【30】	Debug Uart(4pin 2.0mm)
【31】	GPIO(2*10pin 2,0mm)
【32】	4G Module Slot(PCIE port)
【33】	RK3568 SOM

The board uses 12V DC power supply, that connect by DC 12V Input connector or 4pin 2.54mm 12V Input connector.

Details of other interfaces, could refer to the schematic diagram and layout of the development board.

Chapter 4. Hardware Design

4.1 Design Reference

Take TC-RK3568 Development Board as hardware platform, you could refer to Power design, USB design, PCIE Port design, MIPI display design, Audio design, Ethernet design, Camera design, and so on. These are open to customers, can refer to our carrier board design.

Chapter 5. Software Design

TC-RK3568 develop platform supports Android11, Linux Buildroot, Ubuntu and Debian System OS, source codes are open. You can read the references such as Thinkcore TC-RK3568 system usermanual .